

Design, fabrication and testing of digital signal processing scheme for inertial grade Fiber Optic Gyroscope (FOG)

G. Krishna Prasad and Jagannath Nayak
Inertial System Group,
Research Center Imarath, Hyderabad.

ABSTRACT

Fiber optic gyroscopes are in advance stage of development and currently replacing all conventional gyroscopes in Inertial Navigation Systems (INS).¹ FOG has to be operated in closed loop condition to achieve inertial grade performance. Serrodyne modulation based closed loop signal processing scheme has been simulated and implemented in real time, which includes extraction of optical sagnac phase shift, feedback signal generation and deadband compensation.

The hardware for the closed loop FOG has been developed and tested. Performance is evaluated in terms of bias drift, scale factor accuracy and random walk. Bias drift of 0.1 deg/hr, scale factor accuracy of 800 ppm and random walk of $0.01 \text{ deg/hr}/\sqrt{hr}$ is reported.

Keywords: FOG, closed loop fiber optic gyro, serrodyne modulation

1. INTRODUCTION

Earlier Inertial Navigation Systems (INS) based on mechanical gyroscopes were heavy, complex and of limited bandwidth, dynamic range and reliability. Their reaction time was large and the instrument was difficult to maintain. Optical gyroscopes such as Ring Laser Gyros (RLG) and Fiber Optic Gyros (FOG) are far more superior to their conventional counterparts because of low reaction time, no 'g' sensitivity drift, wide dynamic range, high accuracy and reliability which is the need for modern inertial navigation systems. These problems lead to very low production rate and hence the high cost. However RLG is a complex technology challenge as it needs very good quality optical components. It also has a problem of dead zone because of coupling between backscattered light with counter rotating beams.

Fiber optic gyro technology has support from two growing fields namely, fiber optic communication and silicon technology. These components proved to be the key factor in the development of Fiber Optic Gyroscope.

1.1. Basic principle of FOG

Sagnac first demonstrated the optical gyroscope principle in 1913. Optical gyroscopes implemented so far use Sagnac effect, which states that an optical path difference induced by counter propagating beams in a rotating reference frame is proportional to the absolute rotation.

The basic configuration of the Sagnac interferometer and its operation principle is shown in Figure 1. When system is at rest the light propagating in clockwise (CW) and counter clockwise (CCW) directions traverse identical paths and so there is no phase difference between them. When the system rotates at an angular rotation rate Ω , the resultant rotation induced sagnac phase shift $\Delta\phi_R$ is given by²

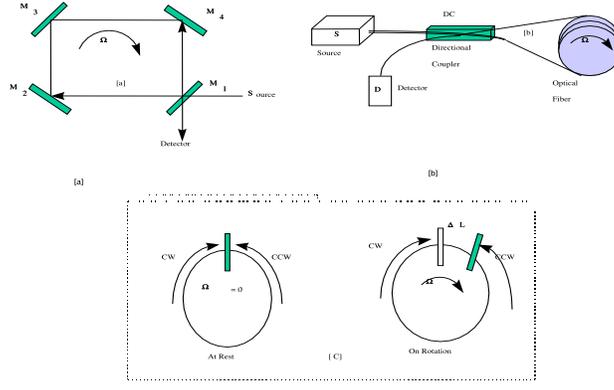


Figure 1. Sagnac Interferometer [a] Bulk Optics [b] Fiber Optics and [c] Simplified interferometer.

$$\Delta\phi_R = \frac{4\pi RL}{\lambda C} \Omega \quad (1)$$

where R is radius of the sensor coil, L is length of the optical fiber, λ is light wavelength, and C is the speed of light in vacuum.

As with any two interferometer where two waves overlap in space, the response obtained is sinusoidal. Thus, the optical intensity can be written as

$$P = P_0(1 + \cos(\Delta\phi_R)) \quad (2)$$

The main limitations of this basic configuration

1. poor sensitivity for small rotation rates.
2. The direction of rotation cannot be determined.
3. Restricted dynamic range due to the 2π periodicity of the response curve.
4. The output is a nonlinear function of the rotation rate.

The problems of poor sensitivity and ambiguity in the determination of direction are usually overcome by the application of the phase modulation. In open loop approach, variations in the returning optical power and changes in the amplitude of the phase modulation will cause errors in output.

1.2. Configuration of closed-loop FOG

The configuration of closed-loop FOG is shown in Figure 2. The rotation rate information $\Delta\phi_R$ is extracted from the detector signal and properly filtered feedback signal is given to an optical feedback element which is placed in the fiber sensing loop. The function of this optical feedback unit is provide a feedback phase shift ϕ_f between the CW and CCW optical waves in the fiber sensing loop proportional to the electrical signal. The feedback loop will adjust the feedback phase shift is always nearly equal and opposite in sign to the Sagnac phase for all constant input rotation rates.³

$$\phi_f = -\Delta\phi_R \quad (3)$$

Equation (3) implies that the total phase shift around the fiber sensing loop is nearly equal zero. Such fiber gyros are also referred to as phase nulling gyros.⁴ The output of the closed-loop fiber gyro is now the electrical signal applied to the feedback element.

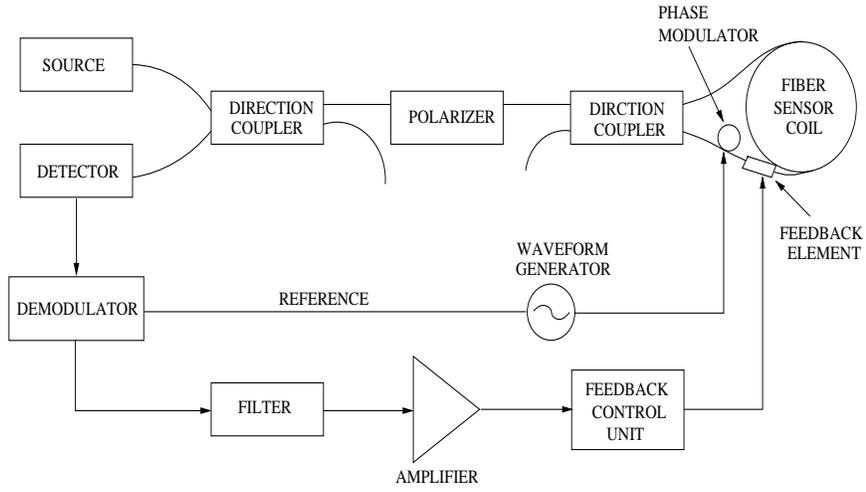


Figure 2. Schematic of a closed-loop fiber gyro

The feedback signal is given in the form of digital ramp (Figure 3) to the optical phase modulator, and slope of the digital ramp is proportional to rotation rate Ω . The duration of each digital step is normally equal to coil transit time, τ . This modulation technique is called as digital serrodyne modulation.

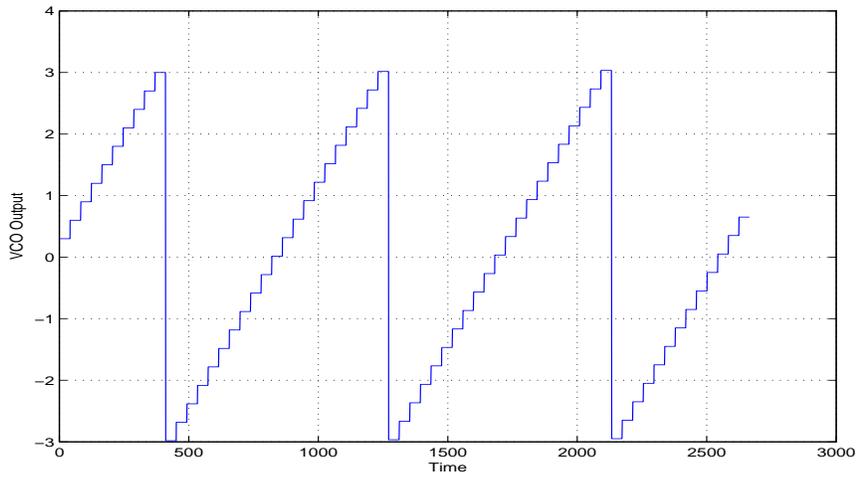


Figure 3. A digital serrodyne signal for $\Omega \neq 0$

$$\phi_f(t) = K_{fp}(V(t) - V(t - \tau)) \quad (4)$$

where $V(t)$ is the instantaneous voltage applied to the feedback modulator and K_{fp} is the modulator constant.

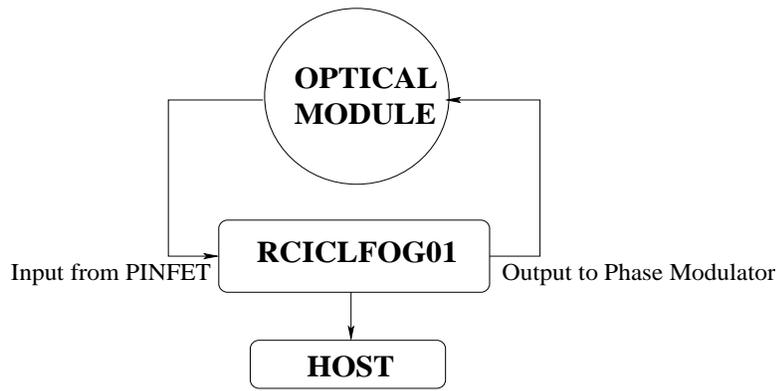


Figure 4. System block diagram

2. HARDWARE IMPLEMENTATION

2.1. System block diagram

Signal processing board (RCICLFOG01) is segmented into four major parts.

1. Signal conditioning amplifier, which will amplify the input PINFET signal to ADC input range.
2. DSP processor, which will read samples from ADC, implementation of closed loop algorithm and write samples to DACs.
3. Optical phase modulator driver, which will give biasing and feedback electrical signal to phase modulator.
4. Digital output driver, which will give digital rotation rate value in RS422 levels.

2.2. Deign Description

2.2.1. DSP Processor

Closed loop FOG dynamic range is about $70dB$, to process these 20-bit values 32-bit processor is required. In this closed loop process ADC reading, demodulation, filtering, serrodyne modulation, writing DAC, 2π reset loop, temperature compensation is more complex. All these operations should be completed within a cycle of modulation frequency. Because of these complexities and high precision signal processing a high performance 32-bit/40-bit floating-point processor is selected.

2.2.2. Analog-to-Digital Converter

For a dynamic range of 70 dB, 20-bit ADC is required. The bandwidth of analog signal is quite large which yields an important white noise. Signal processing theory shows that it is sufficient to sample the analog signal with an LSB just smaller than the σ value of the noise, to get through digital integration the same noise reduction as with analog filtering, without any electronic source of long term drift and dead zone. To achieve the performance 16 bit ADC is selected.

2.2.3. Digital-to-Analog converter

Serrodyne modulation signal is generated by DAC, 14-bit DAC is selected. This serial, current output DAC is having 40ns settling time.

2.2.4. Op-Amp

Closed loop signal processing requires very an exceptionally high performance, high speed, low noise amplifier. The same op-amp is used as an IOC driver circuits for better results.

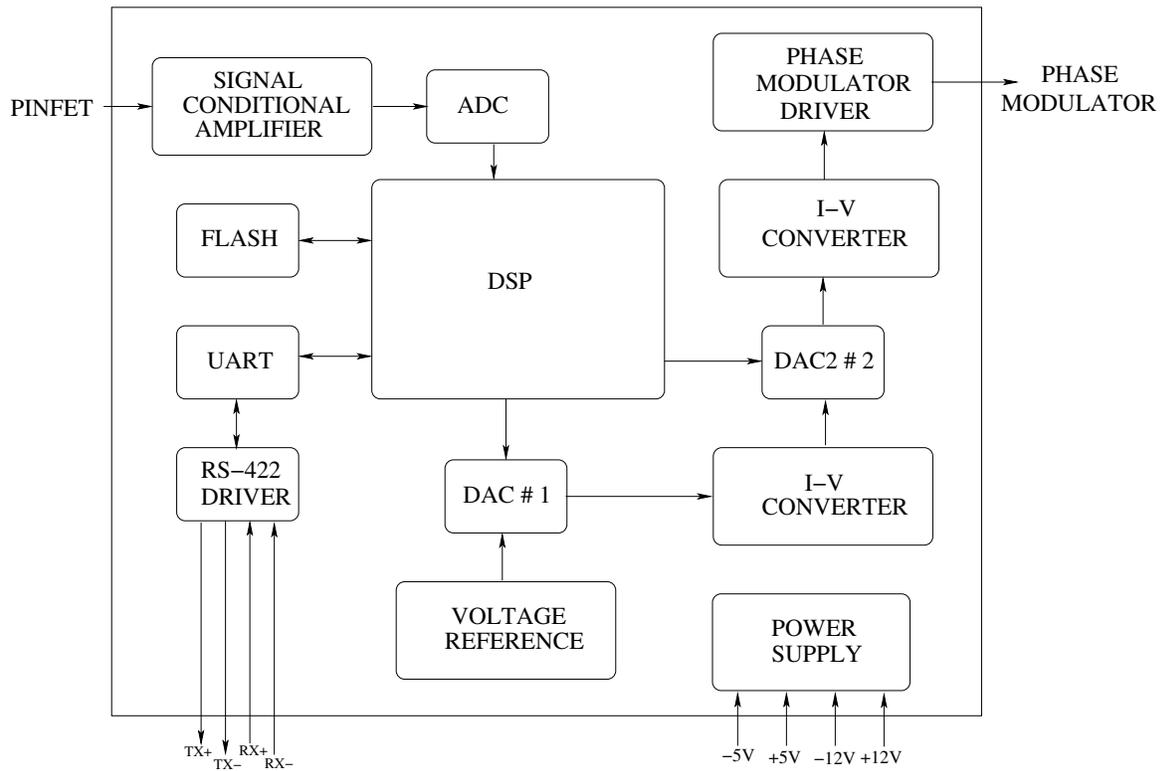


Figure 5. RCICLFOG01 block diagram

2.2.5. Voltage Reference

In the 2π reset loop, voltage reference is required. The IOC driver voltage stability of V_π dependent on the DACs voltage reference. Low temperature coefficient and low noise voltage reference is selected.

2.3. Implementation details

2.3.1. Power supply

The RCICLFOG is having input voltage of $\pm 5V$ and $\pm 12V$, some of the components required different voltages like 1.2V, 2.5V and 3.3V. So these voltages are generated inside the signal processing board.

2.3.2. Flash, UART and RS422

Serial FLASH and UART are connected on the SPI lines shown in figure 5. FLAG0 and FLAG1 are used to selected FLASH and UART. The rotation rate information is sending out in digital form through RS422 interface. This is achieved by connecting output of the UART to RS422 driver, which will give RS422 levels.

2.3.3. Signal conditional amplifier

The PINFET output is converted into differential to drive the ADC.

2.3.4. ADC and Processor interface

The ADC is connected to the parallel port of the processor.

2.3.5. 2π Voltage Controller

The modulator input signal 2π voltage is controlled by the DAC#1. The output of the I-V of DAC# will swing upto $\pm 10V$, the 2π voltages of the IOC is within the 10V. The maximum output voltage of I-V converter(1) will be 10V for a code $3FFF$. Therefore the 2π voltage can be controlled by the software.

2.3.6. Modulator Driver circuit

The biasing and serrodyne signals are added inside the DSP and given out by DAC#1. The DAC#1 is current output and its settling time is 40ns. The voltage swing of the I-V converter is controlled by the digital value written to the DAC#2. The single-ended signal is converted into differential to drive IOC.

3. SOFTWARE DEVELOPMENT

The DSP firmware mainly consists of following 1. Interfacing with ADC, DAC, and external world.
2. Closed loop algorithm (Gyro controller) implementation.

3.1. ADC data processing

The input processor will have temporary storage of the input samples which can be used by the internal Gyro controller.

3.2. DAC Output Processing

The processed data output from Gyro controller will be fed to output FIFO for temporary storage. These samples will be fed to DAC after addition of the reference bias signal (100 KHz square wave).

3.3. UART interface

An UART interface will communicate with external host (PC). The digitized rotation rate values are sent over this communication link.

3.4. Gyro controller

The Gyro controller block diagram is as shown below in figure 6. The demodulator, averager (LPF), Serrodyne generator and bias adder are the modules to be implemented in Gyro controller. The Gyro bias is 100 KHz square wave generated inside the DSP. This bias is added to the serrodyne signal and is fed to the DAC #1.

3.4.1. Demodulator

The variable amplitude error output received, as input to DSP is first fed to demodulator. The demodulated output is then filtered using Low pass filter i.e. average.

3.4.2. Low pass Filter

The low pass filter averages the demodulated error output.

3.4.3. Ramp Generator

The filter output is used to generate the variable period Ramp signal. The filter output is sampled at 100 KHz and then used as step size of ramp.

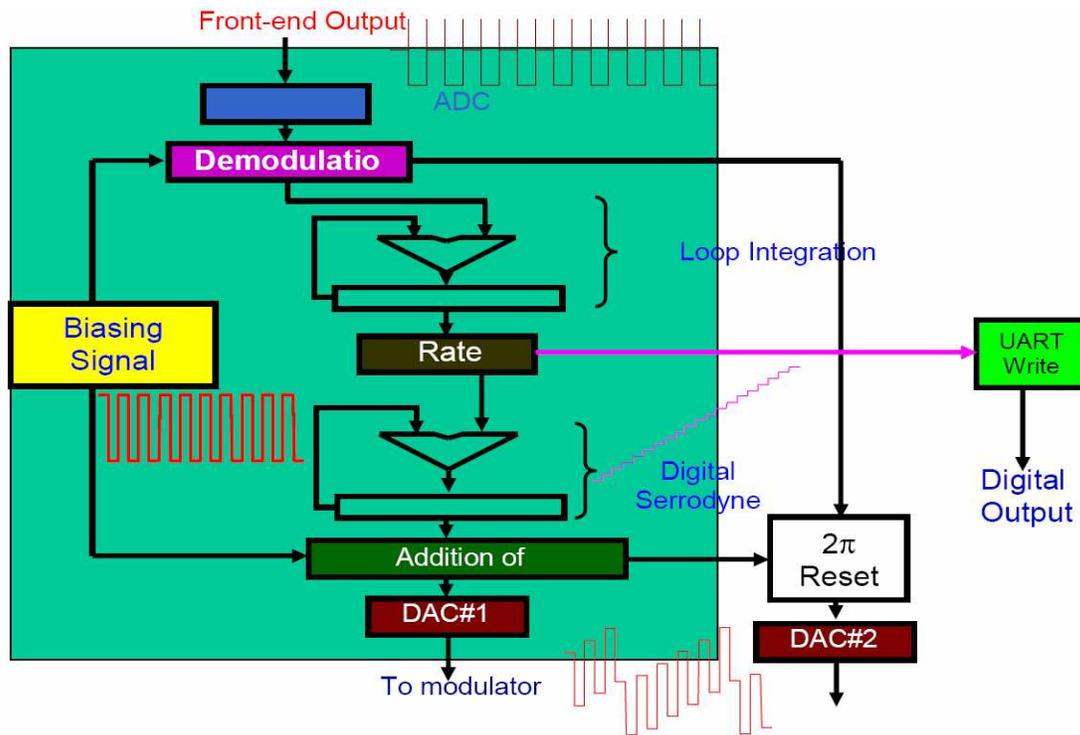


Figure 6. Closed loop FOG signal processing scheme

3.4.4. Adder

The adder adds the serrodyne signal and the biasing reference at 100 KHz square wave.

4. RESULTS

4.1. CLFOG Scale factor

Mount the CLFOG in the fixture on the rate table as shown in the figure 7. Power supply is connected to gyro and data is collection program is started in computer. The power supply is switched ON. Different rotations from -100 deg/sec to + 100 deg/sec is given, each rate duration is 3 minutes and data is collected into PC.

CLFOG scale factor is calculated by computing the slope of the straight line that can be fitted by the method of least squares to the input-output data.

We got scale factor accuracy of 800ppm.

4.2. Bias Drift

Bias drift is a static test, which measured at $\Omega = 0$. By keep CLFOG at $\Omega = 0$ and output from the gyro is captured. Bias drift is calculated by using this equation.

$$\text{Bias Drift} = (\text{Std } (B)/s) * 3600$$

Units: deg/hr

where, B is captured data at $\Omega = 0$ and S is scale factor of the CLFOG.

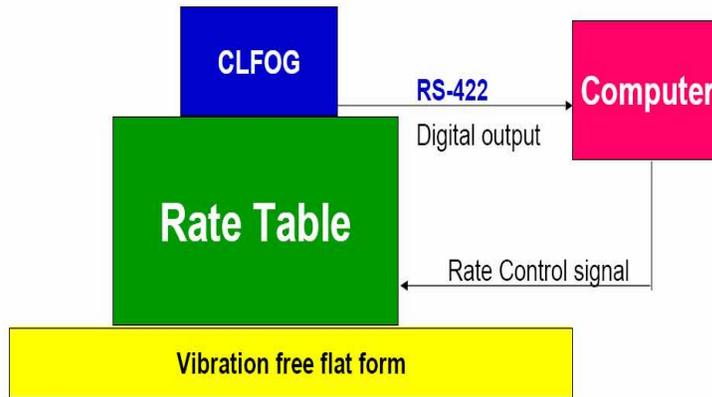


Figure 7. Test setup - Dynamic test

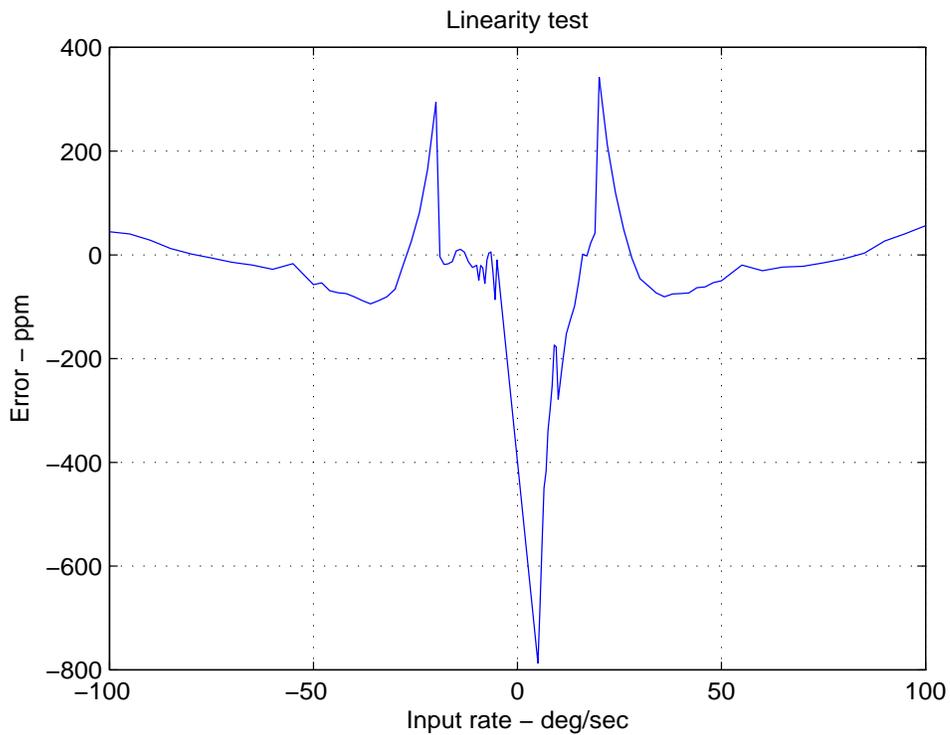


Figure 8. Linearity Test

- Connect the setup as shown in figure 9
- Switch ON power supply.
- Capture the output from the CLFOG for a period of 8 hours.
- Calculate biast drift

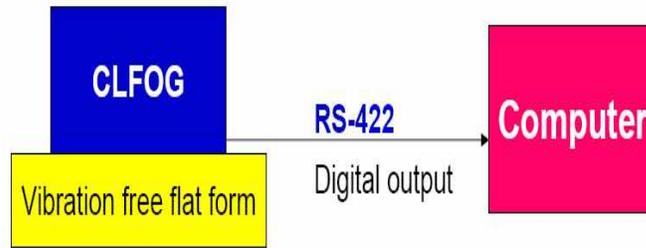


Figure 9. Test setup - Satatic test

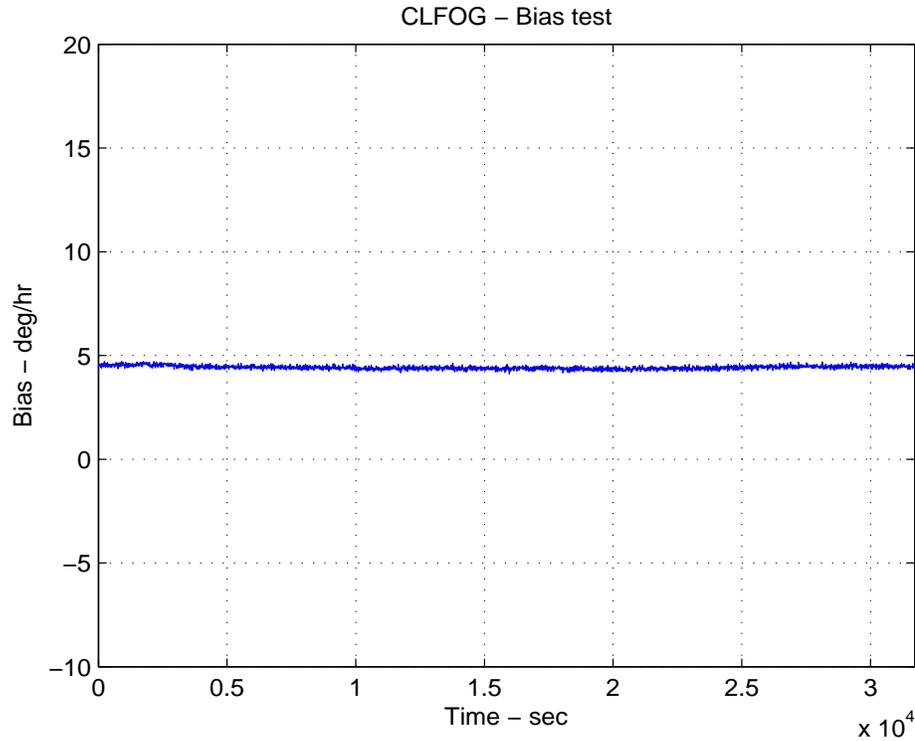


Figure 10. Gyro output when $\Omega = 0$

The static test is carried out 3 days, the repeatability of the closed loop FOG is tested. CLFOG is tested at $\Omega = 0$, the bias drift of the closed loop FOG is 0.1 deg/hr shown in figure 10. By using static test data randomwalk of the CLFOG is calculated as $0.01 \text{ deg}/\sqrt{\text{Hz}}$. We have up-down test, since CLFOG is having bias drift of 0.1 deg/hr it can sense earth rotation. Earth is rotating at 15 deg/hr, at hyderabad earth rotation value is 4.4 deg/hr. By keeping gyro vertically up it has sensed rotation rate 4.4 deg/hr and vertically down sensed as -4.4 deg/hr.

Table 1. Test results of the closed-loop FOG

Bias drift (deg/hr)	0.1
Scale factor accuracy (ppm)	800
Range (deg/sec)	± 100
Random walk (deg/ \sqrt{Hz})	0.01

5. CONCLUSIONS

One prototype of closed loop FOG have been developed and performance evaluated. The bias drift, random walk, scale factor stability and the dynamic range meets the requirement of the navigations specification of the gyros. These prototypes are designed to meet the environmental specifications such as high temperature, low temperature, vibrations, shock, bumps, damp heat and EMI/EMC tests. Structural and thermal analysis of the mechanical package ensures that the package is meeting the environmental specifications. The further work will be to carry out the qualification of the units.

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