Smart Readout for Sensors using FPGA

J.Kamala[*a,] K.R.Ganesh[b], B.Umamaheswari[c]
[a]Dept. of ECE, College of Engg., Guindy, Anna University, Chennai;
[b]Dept. of ECE, College of Engg., Guindy, Anna University, Chennai;
[c]Dept. of EEE, College of Engg., Guindy, Anna University, Chennai;

ABSTRACT

This paper presents a methodology for designing smart readout for sensors using FPGA. The basic components of smart readout are Smart Transducer Interface Module (STIM), Transducer Electronic Data Sheet (TEDS), and Network Capable Application Processor (NCAP). Necessary architecture is proposed to accommodate maximum of functional blocks in the digital platform of FPGA itself with minimum external analog parts ensuring reliability and compactness. The circuit is optimized for fast operation with necessary parallel algorithms. The design is tested for various current sensors applications in this paper for universal implementation, modularity and future expansion. A special architecture for STIM/TEDS is developed.

Keywords: STIM, NCAP, FPGA,TEDS,, Hall effect current sensor

1. INTRODUCTION

This paper presents a method to connect more number of sensors in IEEE1451 standard using FPGA. IEEE 1451 is the IEEE Standard for a Smart Transducer Interface for Sensors and Actuators— Common Functions, Communication Protocols, and Transducer Electronic Data Sheet (TEDS) Formats[6]. This standard is approved on 9 August 2007 by American National Standards Institute and IEEE-SA Standards Board on 22 March 2007. It reduces the complexities in establishing digital communication with transducers and actuators. It defines the bus architectures, addressing protocols, wiring, calibration and error correction, thus enabling a building block approach to system design with plug-and-play modules. This standard introduces the concept of a transducer interface module (TIM) and a network capable application processor (NCAP) connected by a media specified by another member of the IEEE 1451 family of standards.

A TIM is a module that contains the interface, signal conditioning, analog-to-digital and/or digital-to-analog conversion and, in many cases, the transducer. A TIM may range in complexity from a single sensor or actuator to units containing many transducers (sensors and actuators). STIM[4],[7] specified in the IEEE 1451.2-1997 standard (IEEE Standard for a Smart Transducer Interface for Sensors and Actuators Transducer to Microprocessor Communication Protocols and Transducer Electronic Data Sheet - Approved 16 September 1997 by IEEE Standards Board) is referred as TIM in this standard. An NCAP is the hardware and software that provides the gateway function between the TIMs and the user network or host processor.

A standalone HDL model of TIM with integrated TEDS is developed in this work using FPGA. The sensor can be connected to any user network or host processor by programming the target FPGA according to user requirements. A sensor or actuator connected with this proposed architecture is smart, because of three features

- It is described by a machine-readable Transducer Electronic Data Sheet (TEDS).
- The control and data associated with the transducer are digital.
- Triggering, status, and control are provided to support the proper functioning of the transducer.

2. PROPOSED STIM/TEDS ARCHITECTURE

The proposed architecture is a standalone STIM/TEDS architecture using FPGA. The main components are shown in fig.1. The functional elements of the processor need to perform

1. Storage of transducer parameters
2. Algorithm for calibration of transducer using IEEE 1451 standard.
3. Generation of processed output.

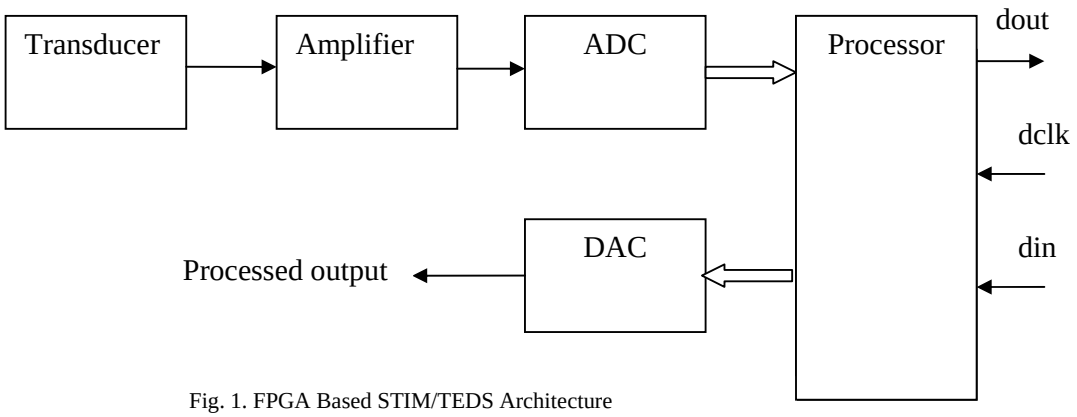

Fig. 1. FPGA Based STIM/TEDS Architecture

Two current sensors namely Differential Amplifier input resistive current sensor and Hall effect current sensors are connected in a network for this application. Differential amplifier input resistive current sensor is implemented with low cost resistors and an operational amplifier. Hall effect current sensor provides an output voltage proportional to input current. These sensors are connected to FPGA using transducer interface module. The FPGA kit implements the IEEE 1451 standard and provides the digital output of the sensors. The FPGA kit comprises Xilinx QPRO Virtex-II XQV100 with interfaces for switches, LEDs, LCDs, ADC, DAC, Keyboard, Mouse and RS232 UART. The block diagram representation of processor is shown in fig.2.

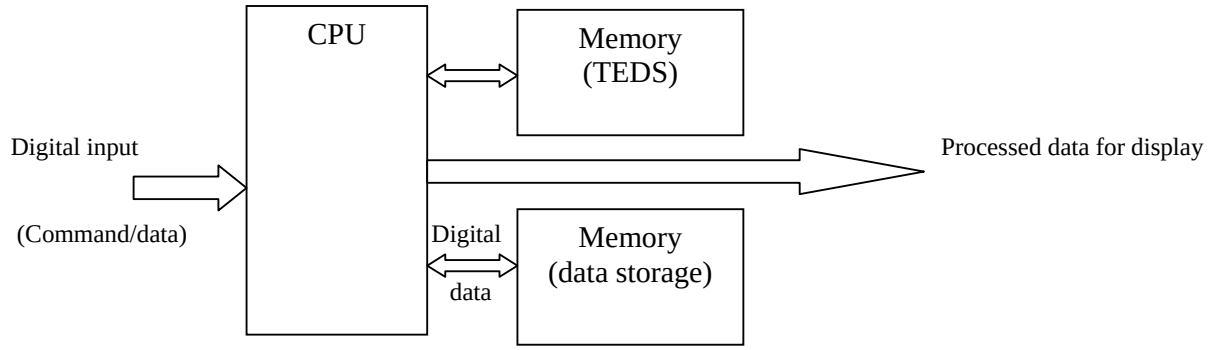

Fig.2 Block diagram representation of Processor Architecture

The FPGA is programmed to implement the commands used in IEEE Std 1451.0-2007. These commands are used to activate the sensors, get the output from sensors and store the details of the sensors in the form of TEDS. TEDS is a set of memory locations used to store the details of sensors, which is also implemented inside the FPGA. Contents of TEDS can be read or updated using commands. ADCs available in the FPGA kit is connected with sensors and the ADCs use I^2C logic for communication. The output from the sensors are applied to a signal conditioning circuit called Smart Transducer Interface Module, which converts the output of the sensor to a form suitable for the input of the ADCs of the FPGA kit. The Smart Transducer Interface Module can be connected to any network through Network Capable Application Processor (NCAP) which can also be implemented in the FPGA. The physical interface between the NCAP and STIM is not described in this standard, therefore for implementation purpose, Serial Peripheral Interface with three communication lines din, dout and dclk are used for data transmission, reception and clock between NCAP and STIM.

2.1 STIM

The signal conditioning circuit used to connect the sensor to a microcontroller is called Smart Transducer Interface Module. STIM is named as TIM Transducer Interface Module in the IEEE Std 1451.0-2007 standard. TIM comprises the circuit associated with the sensor, ADC and DAC channels available in the FPGA kit. The FPGA kit has 4 channels of ADC and one channel of DAC using PCF8591, single chip, single -supply low power 8-bit CMOS data acquisition device with four analog inputs, one analog output and a serial I^2C – bus interface. The functions of the device include analog input multiplexing, on-chip track and hold function, 8-bit analog to digital conversion, and 8-bit digital to analog conversion. Two sensors are connected to the two channels of ADC. The TIM is implemented with two status registers for each transducer channel connected with it They are Condition Register which contains the current state of the attributes being reported. The second register is the event register, and it is true if the condition register has been true since the last time the status-event register was cleared. Both registers are 32-bit in length. The main functional blocks of TIM are sensors, amplifiers, ADCs and TEDS.

2.2 Transducer Electronic Data Sheets

TEDS are blocks of information to be stored in nonvolatile memory within a TIM. If it is not possible to store the TEDS within the TIM, it can be stored in other places of user system, in which case it is called virtual TEDS. As a general rule a TEDS is not changed once the manufacturer or the user establishes the contents of a TEDS. However, it is possible to design Transducer Channels that can change the contents of a TEDS during operation, by making the TEDS attribute bit as adaptive. Four TEDS are required for all TIMs and others are optional. TEDS is implemented with only required TEDS occupying a memory space of 2432 bits. The required TEDS are

Meta-TEDS : It gives some worst-case timing parameters that are available to be used by the NCAP to set time-out values in the communications software to determine when the TIM is not responding. It is stored in memory of size 320 bits.

Transducer Channel TEDS : It gives detailed information about a specific transducer regarding the physical parameter is being measured or controlled, the range over which the Transducer Channel operates, the characteristics of the digital I/O, the operating modes and the timing information. It occupies a memory space of 792 bits.

User's Transducer Name TEDS : It provides a place for the user of the transducer to store the name by which the system will know the transducer. It is stored in a memory of size 104 bits.

PHY TEDS : It is dependent on the physical communication media used to connect the TIM to the NCAP and is not defined in the standard although the method of accessing it is defined.

3. IMPLEMENTATION OF CURRENT TRANSDUCERS

3.1 Differential Amplifier Input Resistive Current Sensor

Current to be measured is passed through a R1 resistor, voltage developed across this resistance is amplified by a differential amplifier. The differential amplifier is designed to have a gain such that the output can be directly connected to the ADC available in the FPGA kit. Important parameters required for this sensor are, for each resistor the temperature coefficient, tolerance and value. Parameters of resistor R1 is crucial in this sensor, which determines the output of the sensor. Differential gain of the amplifier is determined by the other resistors. For the operational amplifier, the required parameters are open loop gain, slew rate, band width, and input impedance. These parameters are used in the calibration of the sensor output by the FPGA .

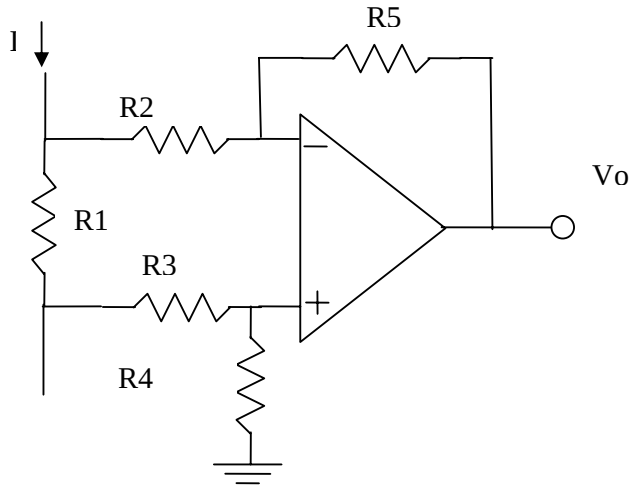

Fig. 3 Differential Amplifier Input Resistive Current Sensor

3.2 Hall Effect Current sensor

HX 10-P/SP2 is the Hall Effect current sensor is another sensor used in our application, which provides an output voltage of 0 to 10V for an input current of 0 to 10A. For this application, the Hall effect current sensor is used to measure the current in the range of 0 to 2.5A. Output of Hall effect current sensor is connected to one channel of ADC available in the FPGA kit. The parameters of the Hall effect current sensor is given below. The parameters related with the transducer are used in the calibration process.

V_{OUT}	Output voltage @ $\pm I_{PN}$, R_L = 2 kΩ, T_A = 25°C	V_{OE} ±0.625	V
R_{OUT}	Output impedance	< 50	Ω
R_L	Load resistance	≥ 2	kΩ
V_C	Supply voltage (± 5 %)	+12 .. +15	V
I_C	Current consumption	< 15	mA
V_d	R.m.s. voltage for AC isolation test, 50/60Hz, 1 mn	> 3	kV
V_e	R.m.s. voltage for partial discharge extinction at 10pC	≥ 1	kV
	Impulse withstand voltage, 1.2/50µs	≥ 6	kV

Terminal Pin Identification

1.....0V
2.....0V
3.....+12V to +15V
4.....Output

5.....Primary input Current(+)
6.....Primary input Current(-)

Fig.4 Parameters related with Hall Effect Current Sensor

4. COMMANDS ISSUED BETWEEN NCAP AND TIM

The control function allows commands to be sent to the TIM as a whole or to each Transducer Channel thereof, that affect their state or operation. The TIM shall respond to all unimplemented commands by setting the TIM invalid command bit in the status register. The commands and the data are transferred through the din and dout lines of Serial Peripheral Interface. Serial bits received in din is checked for a command, accordingly further triggering of a sensor or accessing TEDS/datas are carried out. Fifty six bits are used to represent the commands. The order of transmission of data and command are resolved to the octet level. One octet represents a group of 8 bits. TEDS are represented in the form of octets and hexadecimal number system is used. The commands are implemented using Verilog HDL. The FPGA is programmed to perform the required commands, with five standard command classes, and 18 commands under the command class. The following table illustrates the commands implemented in the FPGA.

Table – 1 : Commands Implemented in the FPGA

Standard Command classes	*Commands*
CommonCmd (Common commands)	Query TEDS, read TEDS, write TEDS, write service request mask, read service request mask, read status event register, write status event register, clear status event register
XdcrIdle (Transducer Idle State)	Address Group definition
XdcrOperate (TransducerOperating state)	Read Transducer channel data-set segment, Trigger command
XdcrEither (Transducer either state)	Transducer channel operate, Transducer channel idle, Read transducer channel trigger state,
TIM Active (TIM Active state)	Read TIM version, Store operational setup, Recall operational setup, Read IEEE1451.0 Version

5. SYNTHESIS REPORT

The Design Entry, Synthesis, and Simulation are done using the Xilinx® Integrated Software Environment (ISE™) 9.2i software, which produces the following synthesis report.

Timing Summary:

Speed Grade: -4

Minimum period: 58.154ns (Maximum Frequency: 17.196MHz)

Minimum input arrival time before clock: 24.153ns

Maximum output required time after clock: 8.498ns

Table 2 :Device Utilization Summary

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1122	1200	93%
Number of Slice Flip Flops	561	2400	23%
Number of 4 input LUTs	2074	2400	86%
Number of bonded IOBs	3	180	1%
Number of GCLKs	1	4	25%

6. SIMULATION RESULTS

The simulation is shown for the command input in the input line din, the command is 56 in hexadecimal for the command query TEDS command. After receiving 56 bits, the command is identified, and the contents of query is placed on the dout output line serially at the rising edge of each clock signal.

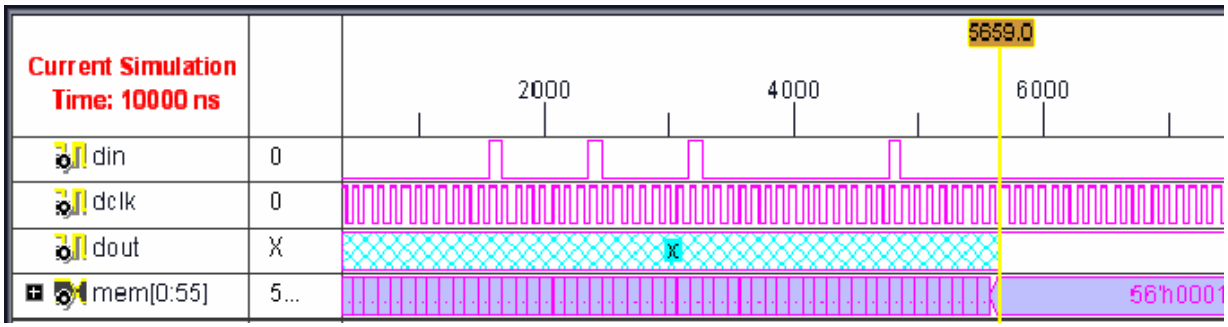

Fig.5 Simulation result for the command : Query TEDS

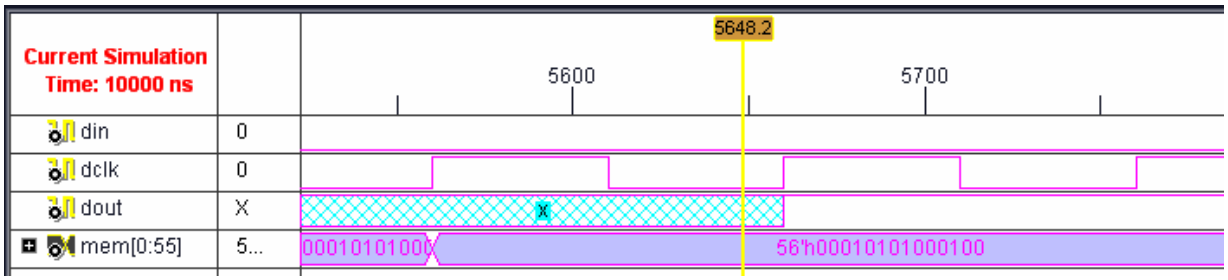

Fig.6 Simulation showing the dout activated after receiving 56 command bits

7. CONCLUSION

This paper shows the implementation of IEEE Std 1451.0-2007 in the FPGA with required commands and TEDS. By choosing higher versions of FPGA, all the optional commands and optional TEDS can be implemented. Otherwise the TEDS can be implemented in other external memories and the FPGA can be fully utilized to perform the command.

Communication with other networks can be implemented by adding external hardware like HP BFOOT 66501 with that it is possible to read and display the TEDS over World Wide Web. A well customized implementation can be realized because only functions related to the specific case are included in the design. This methodology is suitable for high performance of IEEE Std 1451.0-2007 based sensors.

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